

REMARKS

Claims 1-22 are presented for further examination. Claims 1, 2, and 5-18 have been amended. Claims 21 and 22 are new.

In the Office Action mailed February 25, 2003, the Examiner objected to the specification and the claims because of informalities. Applicant has corrected all of the informalities noted by the Examiner with the exception of claim 12, lines 14-15. In this portion of claim 12, the Examiner requested a change from “of other modules in the stack” to “of other stack of modules.” The requested change would render the claim ambiguous, and applicant respectfully requests that the objection to this portion of claim 12 be withdrawn.

Turning to the merits, claims 1-3 and 6-18 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,477,593 (“Khosrowpour et al.”). Claims 4-5 and 19-20 were rejected under 35 U.S.C. § 103(a) as obvious over Khosrowpour et al. in view of U.S. Patent No. 5,707,242 (“Mitra et al.”).

Applicant respectfully disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

The disclosed and claimed embodiments of the invention relate to a stackable module for a processor system. The module includes a support plate with circuit components mounted on the topside. These circuit components constitute a transport stream generating device that is configured to generate transport stream data and transport control signals. According to the present invention, “transport stream data” comprises digital encoded and packetized data conveying audio, video, and other information. The module also includes topside and underside connectors for connecting to other modules and having conductive tracks arranged to convey transport stream data and transport stream control signals between modules in the stack.

Khosrowpour et al., U.S. Patent No. 6,477,593, is directed to a stacked I/O bridge circuit assembly having flexibly configurable connections wherein a motherboard may communicate with two communications channels via the I/O bridge circuits mounted onto daughterboards. Communication from the motherboard to the bridging circuits is via PCI buses that are connected to one or the other of the daughterboards via connectors. The bridging

circuits communicate with the communications channels directly or via the motherboard. Khosrowpour et al. does not teach or suggest transport stream data or a device for generating the same. Rather, Khosrowpour discloses only that buses are provided for the transmission of information, but there is no teaching or suggestion of what form this information may take. While the function of the bridging circuits in Khosrowpour is not described, it is clear that transport stream data is not generated by the circuits.

Mitra et al., U.S. Patent No. 5,707,242, teaches a system and connectors for the electrical interconnection of component boards. The component boards are connected via connectors on the topside and the bottomside of the boards. In Figure 3 of Mitra, the connectors are shown attached to the component boards wherein connections are made between the pins of the connectors and metal pads (29) on the board. Figure 3 also shows how the connector is fixed to the board using pins (24) pushed into holes (27) in the board. This is in contrast to the disclosed embodiments of the present invention, and particularly those embodiments of claims 19 and 20, wherein support pillars are designed to engage one module with the above module, the support pillar *extending from the top surface of the board to engage through a through-hole of another board*. Mitra clearly does not disclose or suggest this feature because there are no support pillars extending from the top surface of the board, and there is no support pillar shown between the modules.

Turning to the claims, claim 1 recites a stackable module for a processor system that comprises a support plate, a set of topside circuit components mounted on a top side of the support plate that constitute a transport stream generating device that generates transport stream data and transport stream control signals. Claim 1 further recites a topside connector mounted to the topside of the support plate; an underside connector mounted to the underside of the support plate; and first and second set of conductive tracks arranged to convey transport stream data and transport stream control signals in the stack of modules. As discussed above, nowhere does Khosrowpour et al. teach or disclose a transport stream generating device configured to generate transport stream data and transport stream control signals. Rather, Khosrowpour discloses only that buses are provided for the transmission of information and there is no teaching or suggestion that this information be transport stream data and transport stream control signals.

Consequently, applicant respectfully submits that claim 1, as well as dependent claims 2-10 are allowable over Khosrowpour et al. Moreover, claims 4 and 5 are also allowable inasmuch as the combination of Khosrowpour et al. and Mitra et al. fail to teach or suggest the claimed combination.

Independent claims 11, 12, and 18 include the limitation discussed above with respect to claim 1 wherein a transport stream generating device is provided that generates transport stream data and transport stream control signals. Inasmuch as Khosrowpour et al. does not teach or suggest transport stream data and transport stream control signals generated by a transport stream generating device on the module, independent claims 11, 12, and 18, as well as dependent claims 13-17 are clearly allowable over the cited reference.

Claims 19 and 20 recite a printed circuit board having conductive surface tracks formed on top and bottom surfaces thereof and pass-through tracks extending through the circuit board. Topside and bottomside connectors are connected to the conductive tracks on the top and bottom sides, respectively, and are connected together via the conductive pass-through tracks. The printed circuit board also has at least *one support pillar extending from the top surface*, and at least one through-hole adapted to receive a support pillar from *another printed circuit board*. Claim 20 further recites the limitation that there is a spacer on the top surface of the printed circuit board to provide clearance. As discussed above, Mitra is not relevant to the present invention because the present invention is not concerned with techniques for attaching connectors to the board as is Mitra et al. Mitra clearly does not teach or suggest a support pillar *extending from the top surface of the board to engage with a through-hole of another board*. This is because in Mitra there are no supporting pillars extending from the top surface of the board and there is no support pillar shown between the modules. Consequently, applicant respectfully submits that claims 19 and 20 are not taught or suggested by the combination of Khosrowpour et al. and Mitra et al.

New claim 21 is directed to a stackable module for a processor system having a support plate with a topside and an underside; a set of topside circuit components mounted on the topside of the support plate that constitute a device that acts on transport stream data and transport stream control signals; topside and underside connectors and first and second sets of

conductive tracks to convey the transport stream data and the transport stream control signals between modules in the stack; and a multiplexor for selectively selecting transport stream data from a lower module in the stack and an upper module in the stack for acting on by the device. Claim 21 is limited to include a multiplexor for selectively selecting the transport stream data from a lower module and an upper module. This provides greater versatility as each module in a stack of modules may receive data from a choice of sources, Khosrowpour et al. discloses no such multiplexor and does not teach or suggest that either of the daughterboards is able to receive data from anything other than the motherboard. Applicant submits that claim 21 is allowable.

Claim 22 recites a stackable module for a processor system that includes a support plate, a set of topside circuit components mounted on the support plate, a topside connector and an underside connector, and first and second sets of conductive tracks configured to convey transport stream data and transport stream control signals between modules in a stack of modules, and the circuit components constituting a device that does not utilize transport stream data and the transport stream control signals with all of the transport stream data and the transport stream control signals being supplied via the topside and underside connectors directly to another module in the stack of modules. Claim 22 is limited to a stackable module in which the circuit components constitute a device that does *not* utilize the transport stream data and transport stream control signals. Therefore, all of the signals are supplied directly to another module in the stack. Again, the conductive tracks are arranged to convey transport stream data and transport stream control signals, which is not taught or suggested by Khosrowpour et al. Moreover, in claim 22 it is recited that all of the signals are supplied directly to another module. In Khosrowpour et al., one of the buses is directed straight to another module; however, a second bus is always supplied to the on-board circuitry of a module. Therefore, Khosrowpour et al. does not disclose that all of the signals are supplied directly to another module. In view of the foregoing, applicant submits that claim 22 is clearly allowable.

In view of the foregoing, applicant submits that all of the claims in this application are now in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously

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resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

Paul Evans

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